

CLAIMS

1. A lateral bipolar CMOS integrated circuit comprising:

5 an inverter circuit comprising an n-channel MOS transistor and a p-channel MOS transistor, and having four terminals of:

a gate input terminal V_{in} connected with the gates of the n-channel MOS transistor and the p-channel MOS
10 transistor;

an output terminal V_{out} connected with the drains of the n-channel MOS transistor and the p-channel MOS transistor;

a p-type base terminal connected with a p-type
15 substrate of the n-channel MOS transistor; and

an n-type base terminal connected with an n-type substrate of the p-channel MOS transistor,

wherein the n-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the
20 MOS transistor and an operation mode of an npn lateral bipolar transistor which is inherent in the n-channel MOS transistor, and

the p-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS
25 transistor and an operation mode of a pnp lateral bipolar

transistor which is inherent in the p-channel MOS transistor.

2. The lateral bipolar CMOS integrated circuit
5 according to claim 1, wherein the gate input terminal V_{in} , the p-type base terminal and the n-type base terminal are input terminals of the inverter circuit, and the output terminal V_{out} is an output terminal of the inverter circuit, and

10 the inverter circuit outputs, at the output terminal V_{out} , a high-level or low-level voltage fed to the gate input terminal V_{in} as an inverted level voltage.

3. The lateral bipolar CMOS integrated circuit
15 according to claim 2, comprising a current source I_{bp} connected with the p-type base terminal of the n-channel MOS transistor and a current source I_{bn} connected with the n-type base terminal of the p-channel MOS transistor,

wherein currents from the current source I_{bp} and the
20 current source I_{bn} are maintained at 0 when the input voltage to the gate input terminal V_{in} is approximately constant at a high level or low level,

when the input voltage to the gate input terminal V_{in} switches from the low level to the high level, a forward
25 pulse current flows from the current source I_{bp} to the p-

type base terminal in synchronization to switching, and

when the input voltage to the gate input terminal V_{in} switches from the high level to the low level, a forward pulse current flows from the current source I_{bn} to the n-type base terminal in synchronization to switching.

4. The lateral bipolar CMOS integrated circuit according to claim 3, further comprising a voltage source V_{dd} and a ground source Gnd ,

wherein the current source I_{bp} is formed by a pull-up p-channel MOS transistor comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the p-type base terminal, and the source terminal and the substrate terminal are connected with the voltage source V_{dd} , and

the current source I_{bn} is formed by a pull-down n-channel MOS transistor comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the n-type base terminal, and the source terminal and the substrate terminal are connected with the ground source Gnd .

5. The lateral bipolar CMOS integrated circuit according to any one of claims 1 through 4,

wherein the inverter circuit comprising the n-channel

MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell.

5